REMARKS

The Examiner's Action mailed on December 24, 2008, has been received and its contents carefully considered.

In this Amendment, Applicant has editorially amended the specification and amended claim 1. Claim 1 is the sole independent claim pending and under consideration, and claims 1, 2 and 4 remain pending and under consideration in the application, claims 3 and 5-17 having been previously withdrawn in response to the Restriction Requirement of November 3, 2008, although claim 3 has been deemed by the Examiner to be directed merely to a different species of the elected invention, and is thus subject to possible rejoinder. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1-4 were rejected as anticipated by *Hirota* (JP 06-268162 A). This rejection is respectfully traversed.

Hirota discloses a semiconductor device having an ordinary-breakdown-strength MOS transistor **30** and a high-breakdown-strength MOS transistor **11** both formed on a semiconductor substrate **10**. However, a LOCOS isolation structure using a field oxide film **33** is applied to both the regions around the ordinary-breakdown-strength MOS transistor **30** and around the high-breakdown-strength MOS transistor **11**.

According to the present invention, on the other hand, an STI (Shallow Trench Isolation) structure is adopted for the first region including the device with

the lower breakdown voltage, while a LOCOS structure is adopted for the second region including the device having the higher breakdown voltage. Thus, the present invention is structurally different from *Hirota*. See the present specification as filed, e.g. ¶¶[0036] and [0069]:

> **[0003]** With this arrangement, so-called shallow trench isolation (STI) is employed for the device isolation in the first region formed with the first device of the lower breakdown voltage, so that the microminiaturization of the structure in the first region can be advantageously achieved. On the other hand, the second device of the higher breakdown voltage formed in the second region has the drift drain structure with the LOCOS oxide film provided at the edge of the gate electrode, so that the problem of the concentration of the electric field can be suppressed which may otherwise occur when a thick insulation film of an STI portion is disposed on the edge of the gate electrode. Thus, the second device has a sufficient breakdown voltage.
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> **[0004]** The lower breakdown voltage transistors **51** formed in the first region **50** are respectively disposed in device formation regions **53** isolated by a shallow trench isolation (STI) portion **52** formed in a surface of the silicon substrate **40**. The STI portion **52** is formed by filling silicon oxide **55** in a shallow trench **54** (e.g, having a depth of about 4000Å) formed in the surface of the semiconductor substrate **40**.

In order to make the structural difference clear, claim 1 has been amended to clarify the STI structure. More specifically, claim 1 has been amended to clarify that the surface of the device isolation portion and the surface of the semiconductor substrate are flush with each other, i.e., the surfaces are in the same plane.

The structure of the device according to *Hirota* is shown in Drawing 1 thereof, from which it is apparent that the field oxide film **33** is not flush with a surface of the substrate, but instead stands proud therefrom, i.e. the field oxide

film **33** does not have a surface in a common plane with a surface of the substrate. This follows directly because the field oxide film **33** has been made by local oxidation, i.e. by a LOCOS process, and not by filling a trench, whereas in the present invention the device isolation portion is made by filling a trench until it is flush with the substrate.

Hirota thus fails to teach or suggest a semiconductor device comprising "a first region defined on the semiconductor substrate and having a first device formation region isolated by a device isolation portion formed by filling an insulator in a trench formed in the semiconductor substrate, wherein *a surface of the device isolation portion and a surface of the semiconductor substrate are both arranged in a common plane*", where the semiconductor device is arranged so as to comprise "a first device provided in the first device formation region" and "a second device provided in the second device formation region and having a higher breakdown voltage than the first device" as recited in claim 1.

Consequently, claim 1 patentably defines over *Hirota* and is allowable, together with claims 2-4 dependent therefrom, and as claim 1 is generic it is respectfully requested that the species of withdrawn claim 3 be rejoined with the species of claims 2 and 4, and claim 3 allowed therewith.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No remittance is believed to be due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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